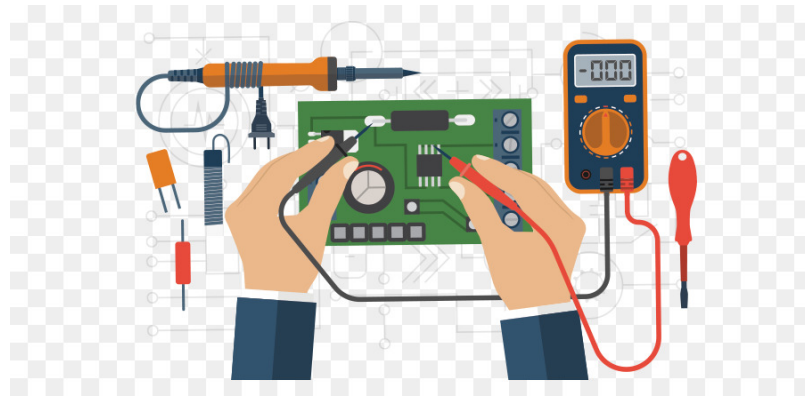


# PANDAVESWAR COLLEGE

## DEPARTMENT OF PHYSICS



### 30 HOURS ADD-ON COURSE IN BASIC ELECTRONICS & DIGITAL LOGIC

# SYLLABUS

## **OBJECTIVE:**

The basic objective of this Course is to provide an insight into the theories, theorems and basics of Electronics and Digital Logic Design. The students would get familiar with Electrostatics, Current Electricity concepts, Semiconductors, Transistors and all types of Circuits (both Combination and Sequential). In the course, numerical problems solving and circuit designing would also be looked into. The knowledge acquired by students through such a course will enable them to prepare in a better manner for PG Entrance examinations and would also help them in Campus interviews (of not only IT companies but also Electrical Engineering companies).

## **DURATION:**

30 Hours add-on course (where one class (lecture): 1 hour, two classes per week).

## **SYLLABUS STRUCTURE OF THE ADD-ON COURSE:**

MODULE	MODULE TITLE	HOURS
MODULE 1	ELECTROSTATICS	4
MODULE 2	CURRENT ELECTRICITY	5
MODULE 3	ELEMENTARY PHYSICS OF SEMICONDUCTORS	8
MODULE 4	DIGITAL SYSTEM DESIGN	10
MODULE 5	TUTORIAL CLASS	3
TOTAL		30

## **SYLLABUS OUTLINE:**

### **MODULE 1: ELECTROSTATICS [TIME: 4 HOURS]**

Coulombs law, Unit of charge, Electric field, Electric lines of force and their properties, Electric flux, Electric potential and potential difference, Gauss law (statement only), Application of Gauss law to find electric field due to a charged sphere, Capacitor and its working, Types of capacitors, Capacitance and its units, Capacitance of a parallel plate capacitor (formula only), Series and parallel combination of capacitors formula (related numerical problems), Dielectric and its effect on capacitance, Dielectric break down.

### **MODULE 2: CURRENT ELECTRICITY [TIME : 5 HOURS]**

Electric Current and its units, Direct and Alternating current, Resistance and its units, Specific Resistance, Conductance, Specific conductance, Series and Parallel combination of Resistances, Factors affecting Resistance of a wire, Carbon Resistance and Colour Coding. Ohm's law, Kirchhoff's laws, Wheatstone bridge, Carrey Foster Bridge and its applications, Concept of Terminal Potential Difference and Electromotive force (EMF), Heating effect of current, Electric power, Electric Energy and its units (related numerical problems), Thermoelectric effect - Seebeck & Peltier effects, Thevenin's & Norton's Theorems (without proof) in Resistive network only & its simple applications.

### MODULE 3: ELEMENTARY PHYSICS OF SEMI-CONDUCTORS [TIME: 8 HOURS]

Intrinsic and Extrinsic semiconductors, P & N type, Diode & its applications: P-N Junction diodes, Biasing of a junction diode, Depletion region & its effect, Zener diodes & its applications, Diode as a rectifier, Types of diodes, LED, LCD, Principle of junction transistor, Current components of transistor, Modes of a transistor (CB, CE and CC) and their properties, I/O characteristics of a transistor in CE mode. Relation between  $\alpha$  &  $\beta$ -parameters of Transistor, Biasing of a transistor - Q point, Load line, Self-bias, fixed bias & collector to base bias.

Amplifiers: Concepts, Class A & B.

Inverters using Transistors – transfer characteristics and threshold voltages. Switching characteristics of diodes and transistors - SCR & UJT.

Principle of FET and MOSFET, Depletion and Enhanced modes of operations, Characteristics and definition of different parameters, Symbols and Application for switching functions, Concept of NMOS, PMOS and CMOS switch.

### MODULE 4: DIGITAL SYSTEM DESIGN [TIME: 10 HOURS]

*Combinational Circuits:* Realization of AND, OR Gates using diodes and NOT Gate using transistors, Standard Gate Assemblies, IC chips packaging nomenclature, Half and Full Adder (3 & bit), Multi-bit adders – Ripple carry and Carry Look Ahead Adder, Adder/Subtractor, BCD-Adder, Data selectors/multiplexers – expansions, reductions, function realization, universal function realization, multi-function realization, Decoders: function realization, De-multiplexer and function realization, Encoder, Priority Encoder, Parity bit Generator/checker, Gray Code Generator, Code Converters, Keyboard encoder, Seven segment display unit, Comparators.

*Sequential Circuits:* Model of Sequential computing, Difference between Combinational and Sequential circuit, RS-Latch: using NAND and NOR Gates, RS Latch as a Static RAM Cell, Problems of Basic Latch circuits, Digital Clock – Duty Cycle, Rising time, Falling time, Clocked Flip Flops - SR, JK, D, T, Level Trigger and Edge Trigger, Excitation Functions of each flip-flops, Flip-flops with Preset and Clear, Application of Flip-flops: Asynchronous Counter (UP/DOWN) upto 4-bit counter, Decade Counter, Mod - n Counter, Finite State machine Model – State Transition Diagram and Table, Synchronous Counters – different mod counters, Ring counter, Johnson's Counter, Registers, Registers with parallel load, Shift Registers.

### MODULE 5: TUTORIAL [TIME: 3 HOURS]

#### LEARNING RESOURCES

SL. NO.	TITLE OF THE BOOK	AUTHOR(S)	PUBLISHER
1	A Textbook of Electrical Technology	B.L. Theraja and A.K. Theraja	S.Chand
2	Modern Digital Electronics	RP Jain	Tata McGraw-Hill Education

3	Basic Electronics, Electricity & Electronics	T.C.Tayal	HimalayaPublishing
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## LESSON PLAN

LECTURES	CONTENT
LECTURE-1(1HOUR)	Coulombslaw,Unitofcharge,Electricfield, Electric lines of force and their properties, Electricflux,Electricpotentialand potential difference
LECTURE-2(1HOUR)	Gauss law (statement only), Application of Gausslaw to find electric field due to a charged sphere,
LECTURE-3(1HOUR)	Capacitor and its working, Types of capacitors,Capacitanceanditsunits,Capacitanceofaparallel platecapacitor(formula only)
LECTURE-4 (1HOUR)	Seriesandparallelcombinationofcapacitorsformula (related numerical problems), Dielectricanditseffectoncapacitance,Dielectricbreak down.
LECTURE-5(1HOUR)	ElectricCurrentanditsunits,DirectandAlternatingcurrent,Resistanceanditsunits,SpecificResistance,Conductance,Specificconductance, Series and Parallel combination ofResistances,FactorsaffectingResistanceofawire, CarbonResistanceand Colour Coding.
LECTURE-6(1HOUR)	Ohm's law, Kirchhoff's laws and applications.
LECTURE-7(1HOUR)	Wheatstone bridge,Carrey Foster Bridge and its applications, ConceptofTerminalPotentialDifferenceandElectromotiveforce(EMF)
LECTURE-8 (1HOUR)	Heatingeffectofcurrent,Electricpower,Electric Energyanditsunits(relatednumericalproblems),Thermoelectriceffect -Seebeck&Peltiereffects
LECTURE-9 (1HOUR)	Thevenin's&Norton'sTheorems(withoutproof) in Resistive network only& it's simpleapplications.
LECTURE-10(1HOUR)	IntrinsicandExtrinsicsemiconductors,P&Ntype,Diode&itsapplications:P-NJunctiondiodes, Biasing of a junction diode
LECTURE-11 (1HOUR)	Depletion region & its effect, Zener diodes & itsapplications, Diode as a rectifier, Types of diodes,LED,LC.
LECTURE-12 (1HOUR)	Principleofjunctiontransistor,Currentcomponentsoftransistor,Modesofa transistor(CB,CEandCC)andtheirproperties.

<b>LECTURE-13(1HOUR)</b>	I/O characteristics of a transistor in CE mode. Relation between $\alpha$ & $\beta$ -parameters of Transistor, Biasing of a transistor-Qpoint, Loadline, Self-bias, fixed bias & collector to base bias
<b>LECTURE-14(1HOUR)</b>	Amplifiers: Concepts, Class A & B. Inverters using Transistors – transfer characteristics and threshold voltages.
<b>LECTURE-15(1HOUR)</b>	Switching characteristics of diodes and transistors - SCR & UJT
<b>LECTURE-16(1HOUR)</b>	Principle of FET and MOSFET, Depletion and Enhanced modes of operations, Characteristics and definition of different parameters
<b>LECTURE-17(1HOUR)</b>	Symbols and Application for switching functions, Concept of NMOS, PMOS and CMOS switch
<b>LECTURE-18(1HOUR)</b>	Realization of AND, OR Gates using diodes and NOT Gate using transistors, Standard Gate Assemblies, IC chip packaging nomenclature
<b>LECTURE-19(1HOUR)</b>	Half and Full Adder (3 & bit), multi-bit adders – Ripple carry and Carry Look Ahead Adder, Adder/Subtractor
<b>LECTURE-20(1HOUR)</b>	BCD-Adder, Data selectors/multiplexers – expansions, reductions, function realization, universal function realization, multi-function Realization
<b>LECTURE-21(1HOUR)</b>	Decoders: function realization, De-multiplexer and function realization, Encoder, Priority Encoder
<b>LECTURE-22(1HOUR)</b>	Parity bit Generator/checker, Gray Code Generator, Code Converters, Keyboard encoder, seven segment display unit, Comparators
<b>LECTURE-23(1HOUR)</b>	Model of Sequential computing, Difference between Combinational and Sequential circuit, RS-Latch: using NAND and NOR Gates, RS Latches a Static RAM Cell, Problems of Basic Latch circuits .
<b>LECTURE-24(1HOUR)</b>	Digital Clock – Duty Cycle, rising time, Falling time, Clocked Flip Flops - SR, JK, D, T, Level Trigger and Edge Trigger, Excitation Functions of each flip-flop
<b>LECTURE-25(1HOUR)</b>	Flip-flops with Preset and Clear, Application of Flip-flops: Asynchronous Counter (UP/DOWN) upto 4-bit counter
<b>LECTURE-26(1HOUR)</b>	Decade Counter, Mod-n Counter, Finite State machine Model – State Transition Diagram and Table
<b>LECTURE-27(1HOUR)</b>	Synchronous Counters – different mod counters, Ring counter, Johnson's Counter, Registers, Registers with parallel load, Shift Registers.

**TUTORIAL CLASS -(3 HOURS)**



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## **EVALUATION POLICY FOR THE ADD-ON COURSE**

The basic philosophy behind the Evaluation policy for this 30 Hours Add-on course is to objectively judge the participants (students) whether the concepts were understandable to them or not and whether they could apply these concepts to solve numerical and conceptual problems. The Evaluation would be done through 3 components –

- i) C1–Course-endAssessment-cum-Test(Written /Onlinemode)[TotalMarks:40]
- ii) C2–Viva-voce [Total Marks:5]
- iii) C3–Attendance[TotalMarks:5]

**TotalMarksoftheEvaluationprocesswould be 50.**

At the end of the Course, there would be a Course-end Assessment-cum-Test evaluation and a Viva based on the entire Course syllabus. Attendance Component Marks would be calculated based on the actual Attendance Percentage of the Student during the classes of the Course.

## **TABLE FOR QUALIFICATION**

<b>TOTAL SCORE (OUT OF 50)</b>	<b>GRADE</b>
<b>40 - 50</b>	<b>A – OUTSTANDING</b>
<b>30 - 39</b>	<b>B – EXCELLENT</b>
<b>20 - 29</b>	<b>C – VERY GOOD</b>
<b>BELOW 20</b>	<b>D – FAILED</b>

## **GENERAL RULES AND REGULATIONS**

1. Students must attend and appear for the Course-End Assessment-cum-Test Examination. If any student fails to submit the Course-End Assessment or fails to attend the Course-End Assessment Examination, the particular Student would NOT BE ELIGIBLE FOR CERTIFICATE.
2. Students must attend and appear for the Course-End Viva. If any student fails to attend the Course-End Viva, the particular Student would NOT BE ELIGIBLE FOR CERTIFICATE.
3. Total Marks of Course Evaluation will be 50 Marks.
4. Minimum 50% Marks has to be scored to receive any Certificate. There will be only ONE Attempt allowed for the Course-End Assessment-cum-Test.
5. There will be NO PROVISION for Backlog Clearance.
6. General Rules and Regulations of the College must be followed without any exception.